

# ABSTRACT

A nonvolatile memory has a plurality of memory cells, each of the memory cells having a first and a second source/drain areas, a control gate, and an insulating trap layer disposed  
5 between the control gate and a channel area lying between the first and the second source/drain areas. The trap layer includes a use bit area in proximity to the first source/drain area, for storing data depending on the presence or absence of electric charge to be trapped, and a non-use bit area in proximity to  
10 the second source/drain area, in which the electric charge is trapped while data is held in the use bit area. Preferably, in the state where erasing operation is completed, the non-use bit area is brought into a state where electric charge is trapped therein.